FIG. 1

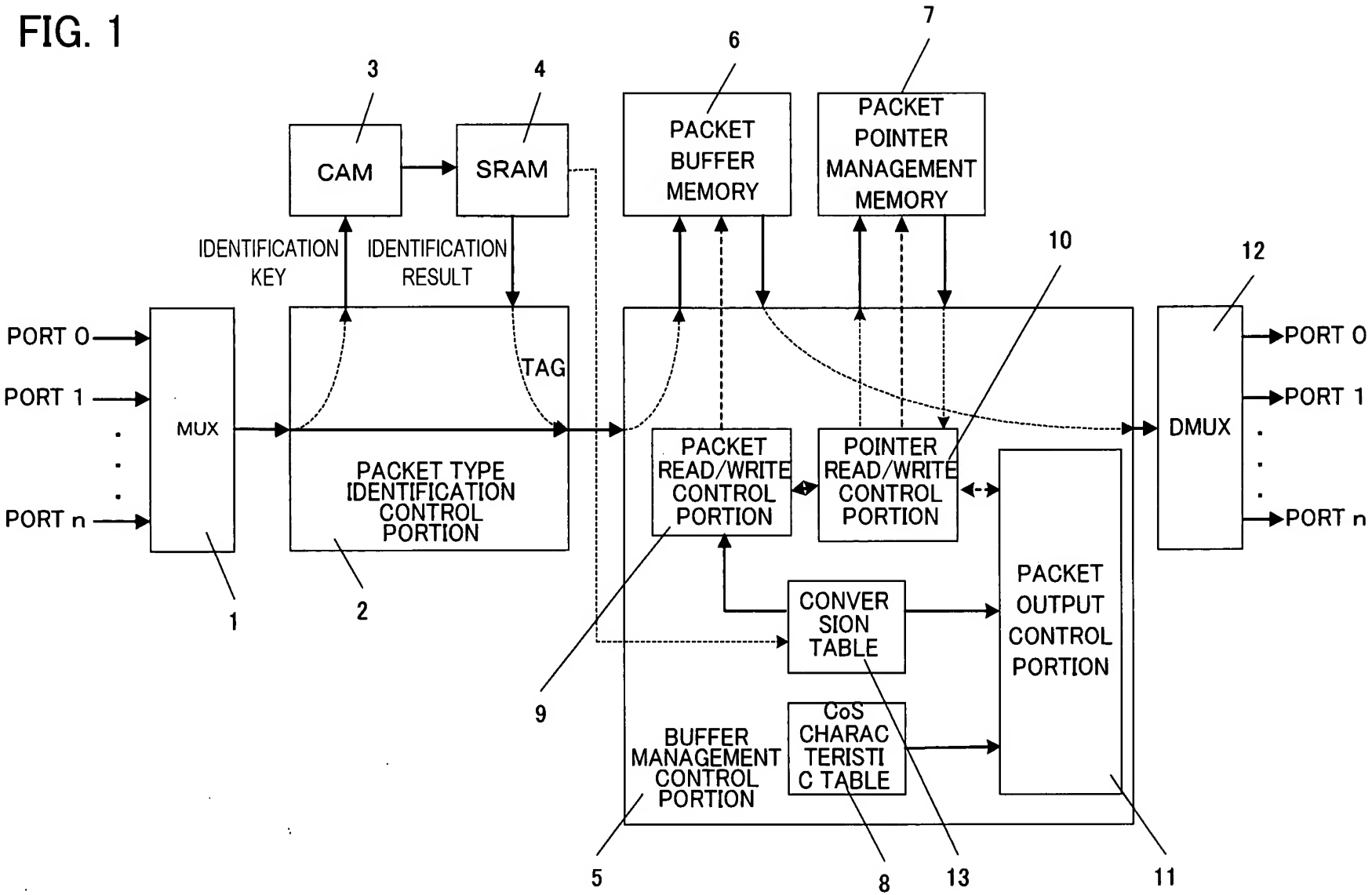

3
4
6
7
CAM
SRAM
PACKET BUFFER MEMORY
PACKET POINTER MANAGEMENT MEMORY
IDENTIFICATION KEY
IDENTIFICATION RESULT
10
12
PORT 0
PORT 1
PORT n
MUX
TAG
PACKET TYPE IDENTIFICATION CONTROL PORTION
PACKET READ/WRITE CONTROL PORTION
POINTER READ/WRITE CONTROL PORTION
DMUX
PORT 0
PORT 1
PORT n
CONVER SION TABLE
PACKET OUTPUT CONTROL PORTION
CoS CHARAC TERISTI C TABLE
BUFFER MANAGEMENT CONTROL PORTION
1
2
9
5
8
13
11

FIG. 2A

FIG. 2B

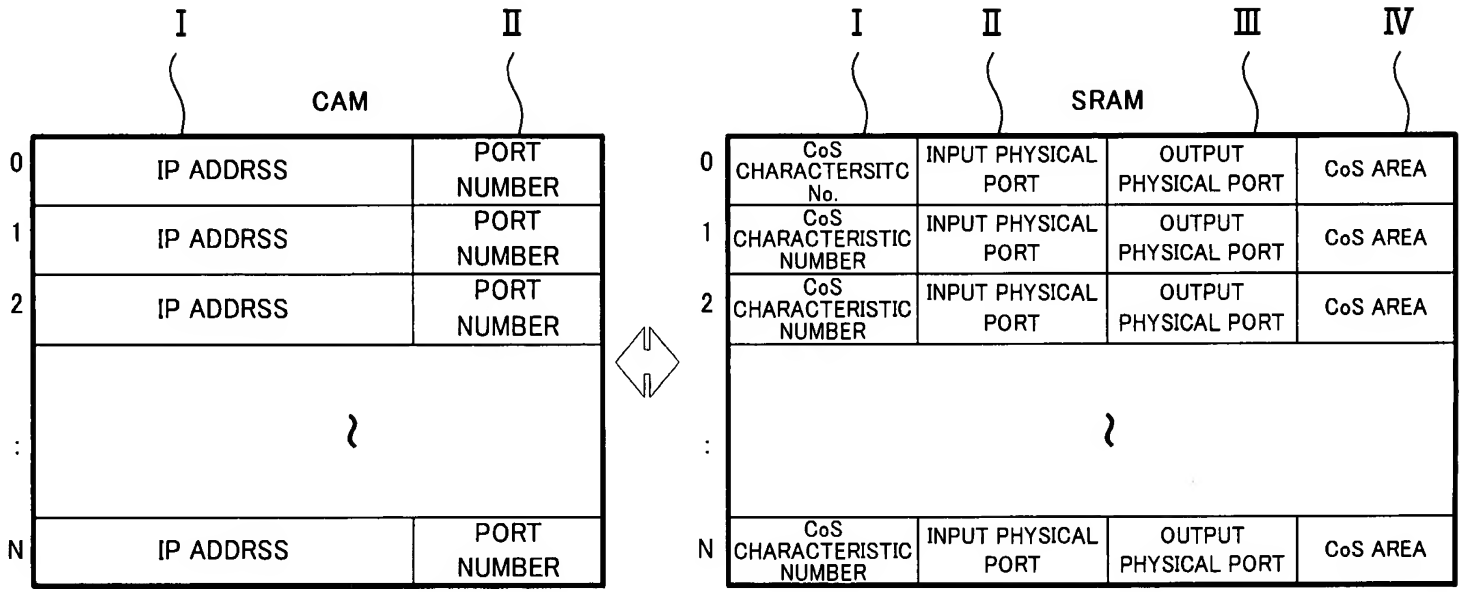


DIAGRAM OF CAM AND SRAM DATA CONFIGURATION

FIG. 3

	(1)	(2)	(3)	(4)	(5)
0	OUTPUT PORT	OUTPUT PORT CoS NUMBER	START ADDRESS	END ADDRESS	CoS CHARACTERISTIC NUMBER
1	OUTPUT PORT	OUTPUT PORT CoS NUMBER	START ADDRESS	END ADDRESS	CoS CHARACTERISTIC NUMBER
2	OUTPUT PORT	OUTPUT PORT CoS NUMBER	START ADDRESS	END ADDRESS	CoS CHARACTERISTIC NUMBER
:	≀				
M	OUTPUT PORT	OUTPUT PORT CoS NUMBER	START ADDRESS	END ADDRESS	CoS CHARACTERISTIC NUMBER

CONVERSION TABLE

FIG. 4

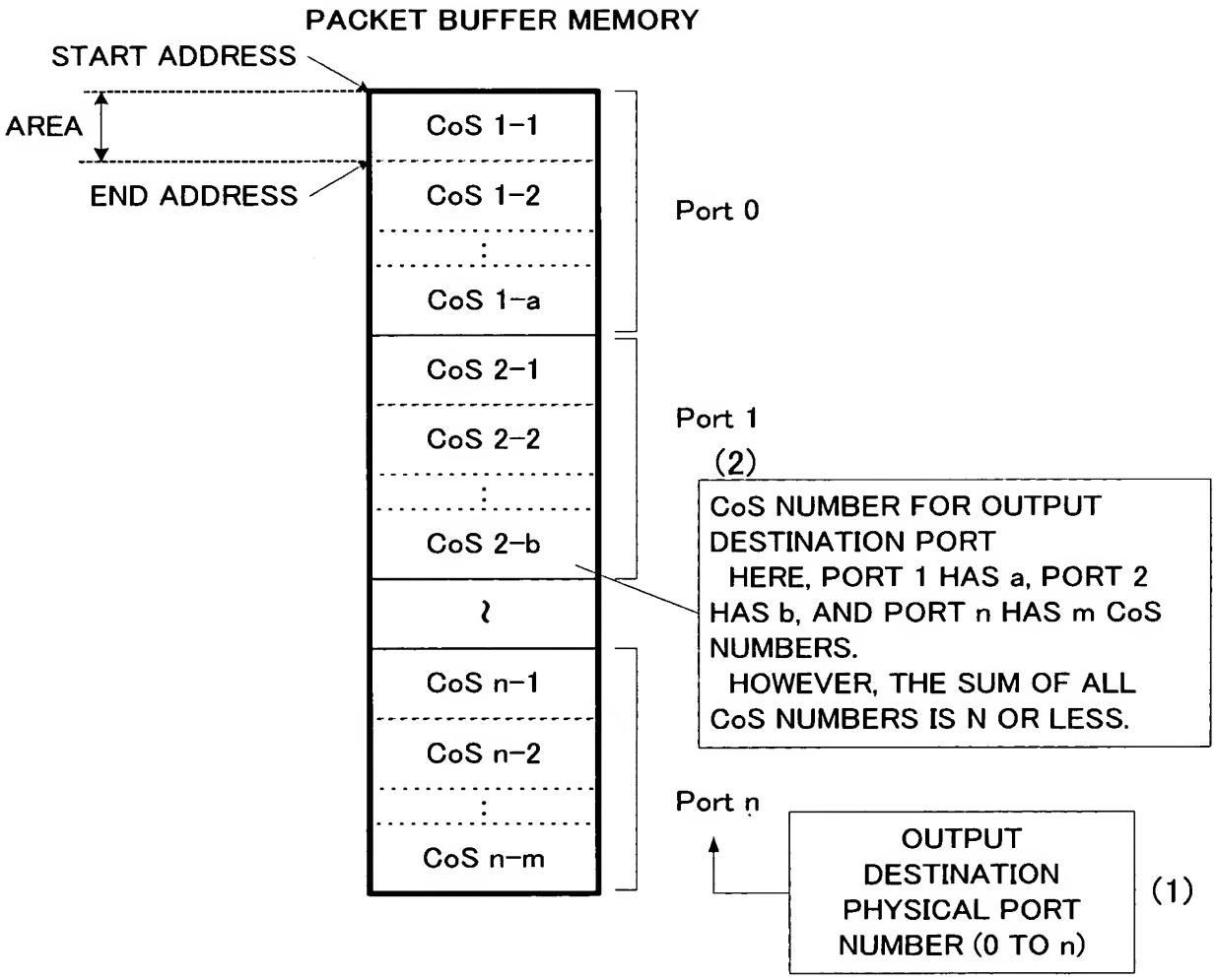


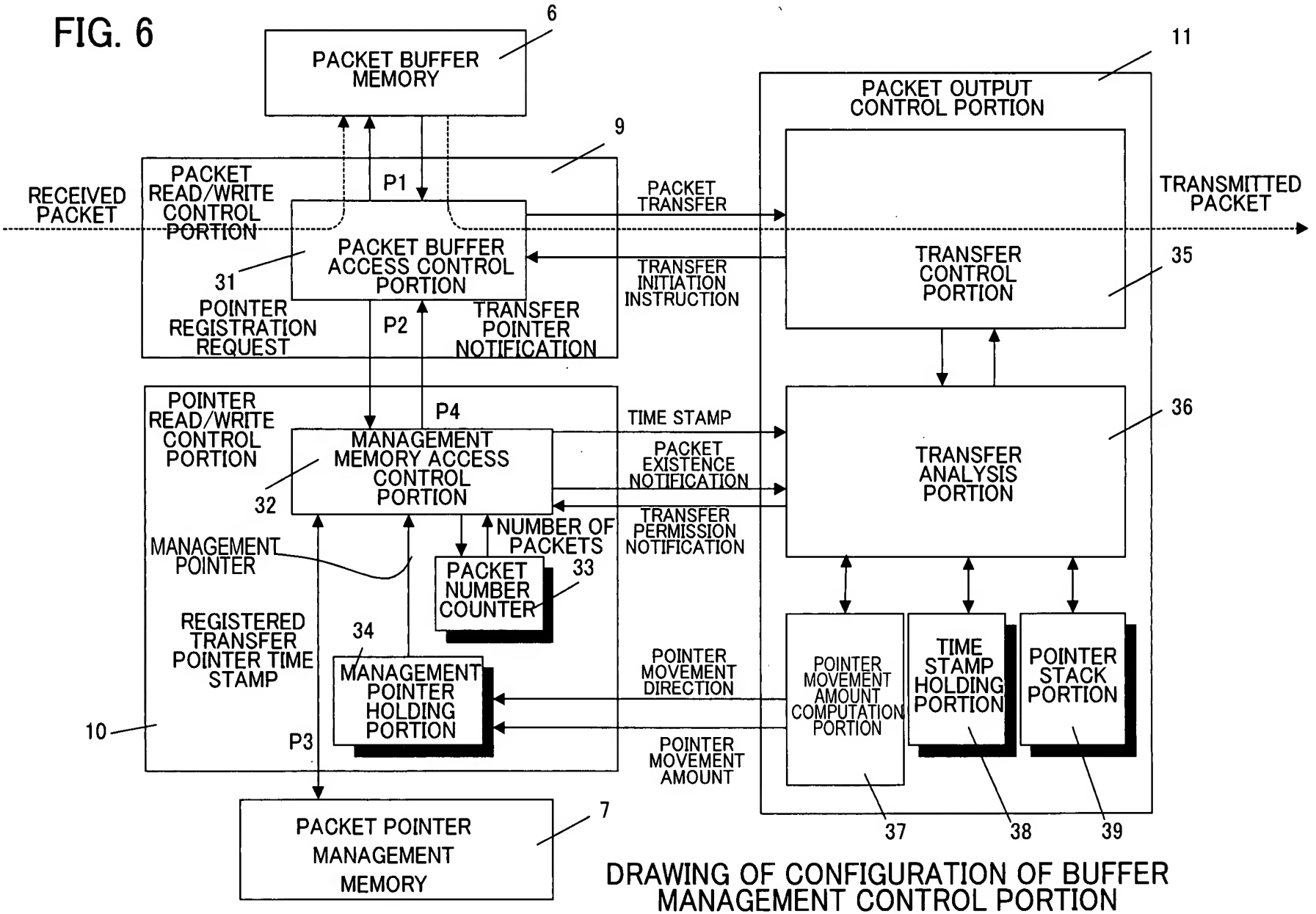
DIAGRAM OF PACKET BUFFER CONFIGURATION

FIG. 5

0	CHARACTERISTIC CONTENTS (LOSS/ERROR INSERTION/DELAY INSERTION/REROUTING ETC)
1	CHARACTERISTIC CONTENTS (LOSS/ERROR INSERTION/DELAY INSERTION/REROUTING ETC)
2	CHARACTERISTIC CONTENTS (LOSS/ERROR INSERTION/DELAY INSERTION/REROUTING ETC)
:	≀
M	CHARACTERISTIC CONTENTS (LOSS/ERROR INSERTION/DELAY INSERTION/REROUTING ETC)

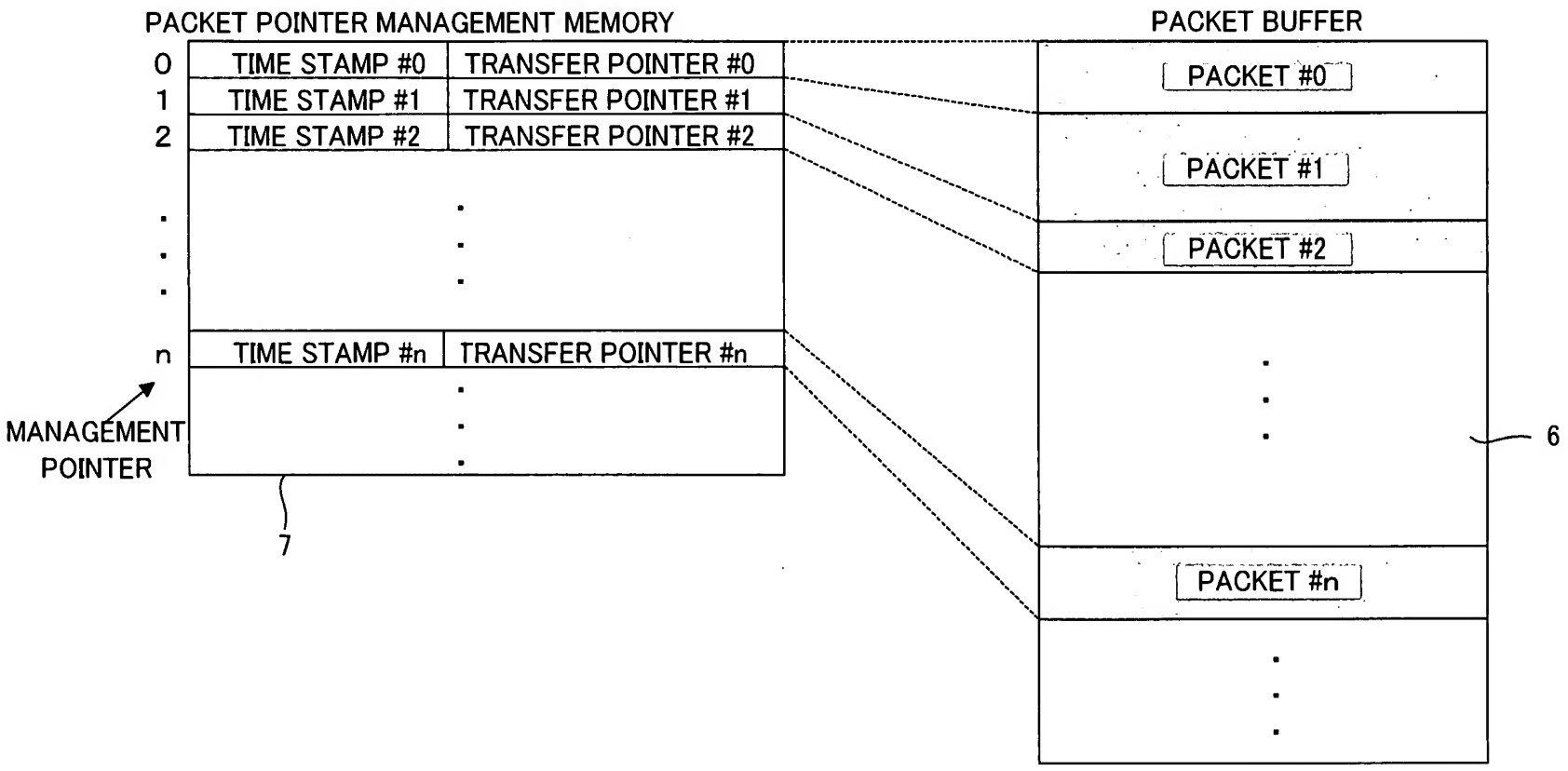
CoS CHARACTERISTIC TABLE

FIG. 6



DRAWING OF CONFIGURATION OF BUFFER MANAGEMENT CONTROL PORTION

FIG. 7



RELATION BETWEEN POINTER MANAGEMENT MEMORY AND PACKET BUFFER

FIG. 8

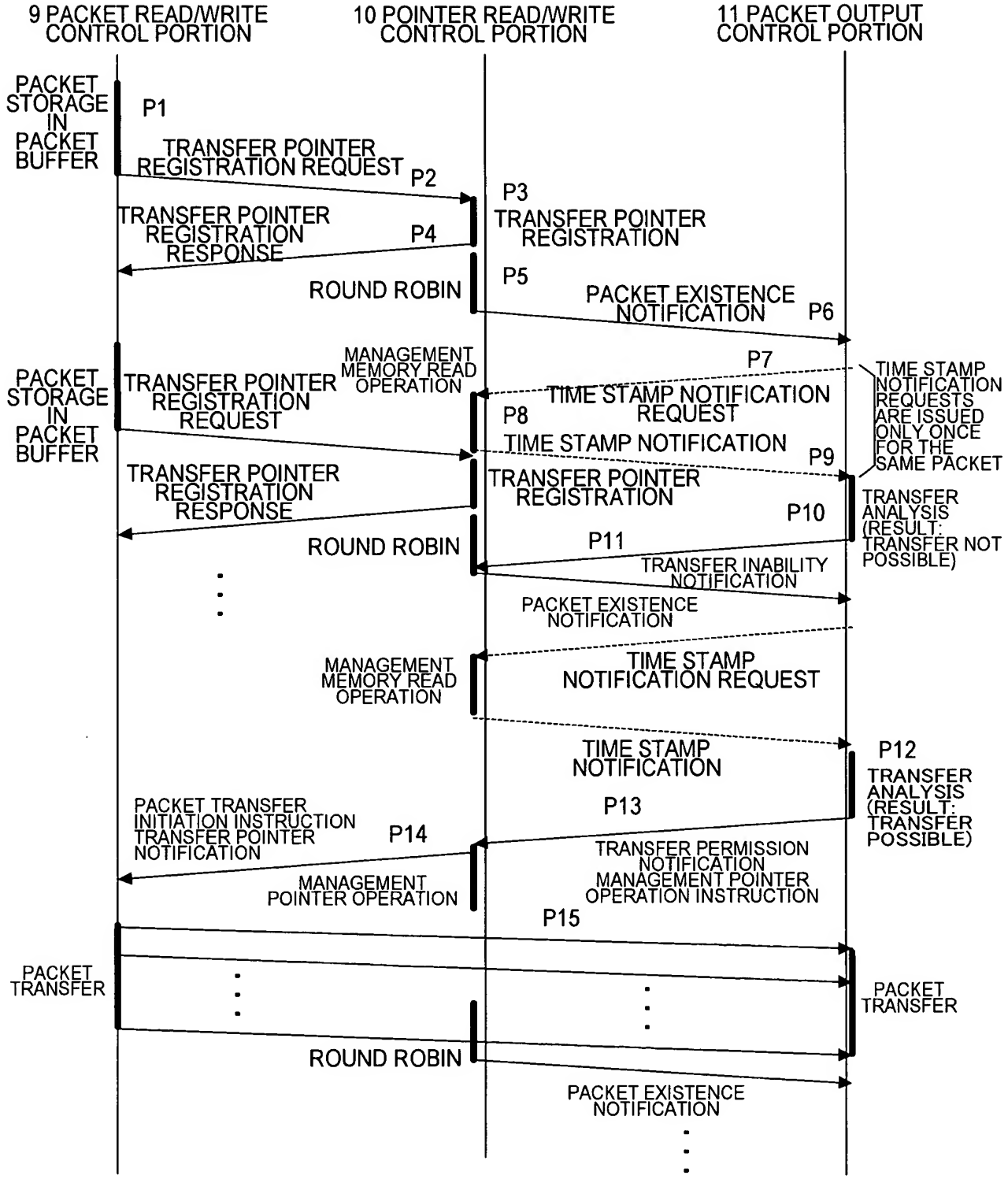
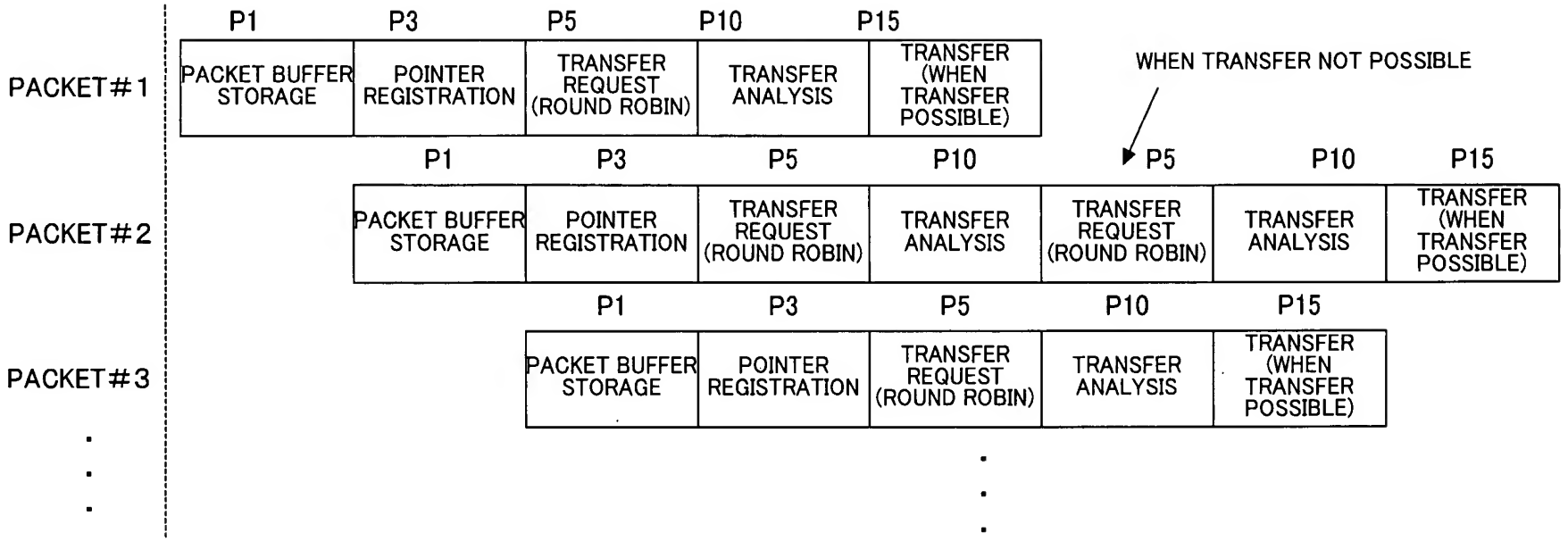
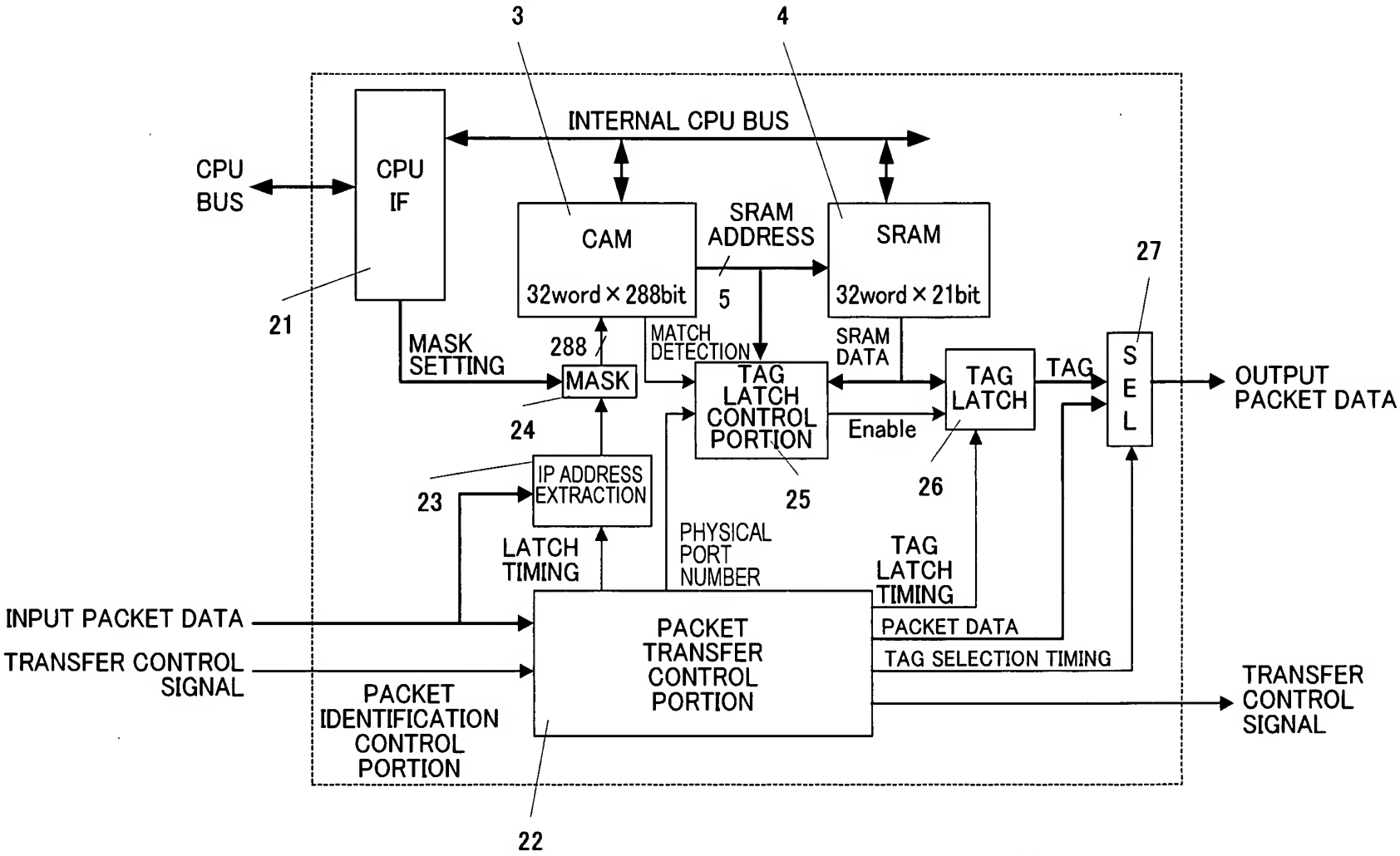

9 PACKET READ/WRITE CONTROL PORTION
10 POINTER READ/WRITE CONTROL PORTION
11 PACKET OUTPUT CONTROL PORTION
PACKET STORAGE IN PACKET BUFFER
P1
TRANSFER POINTER REGISTRATION REQUEST
P2
P3
TRANSFER POINTER REGISTRATION
TRANSFER POINTER REGISTRATION RESPONSE
P4
ROUND ROBIN
P5
PACKET EXISTENCE NOTIFICATION
P6
P7
MANAGEMENT MEMORY READ OPERATION
TIME STAMP NOTIFICATION REQUEST
TIME STAMP NOTIFICATION REQUESTS ARE ISSUED ONLY ONCE FOR THE SAME PACKET
P8
TIME STAMP NOTIFICATION
P9
TRANSFER POINTER REGISTRATION
TRANSFER POINTER REGISTRATION RESPONSE
P10
TRANSFER ANALYSIS (RESULT: TRANSFER NOT POSSIBLE)
ROUND ROBIN
P11
TRANSFER INABILITY NOTIFICATION
PACKET EXISTENCE NOTIFICATION
MANAGEMENT MEMORY READ OPERATION
TIME STAMP NOTIFICATION REQUEST
TIME STAMP NOTIFICATION
P12
TRANSFER ANALYSIS (RESULT: TRANSFER POSSIBLE)
P13
PACKET TRANSFER INITIATION INSTRUCTION TRANSFER POINTER NOTIFICATION
P14
TRANSFER PERMISSION NOTIFICATION MANAGEMENT POINTER OPERATION INSTRUCTION
MANAGEMENT POINTER OPERATION
P15
PACKET TRANSFER
PACKET TRANSFER
ROUND ROBIN
PACKET EXISTENCE NOTIFICATION

FIG. 9



PARALLEL PROCESSING OF BUFFER MANAGEMENT CONTROL

FIG. 10



DETAILED BLOCK DIAGRAM OF PACKET IDENTIFICATION CONTROL PORTION IN ONE EMBODIMENT

FIG. 11A

CAM

ADDRESS	IP ADDRESS (256 BITS)	TCP/UDP PORT NO. (32 BITS)
0	IP ADDRESS 1	PORT NUMBER 1
1	IP ADDRESS 2	PORT NUMBER 2
2	IP ADDRESS 3	PORT NUMBER 3
3	IP ADDRESS 4	PORT NUMBER 4
4	IP ADDRESS 5	PORT NUMBER 5
5	IP ADDRESS 6	PORT NUMBER 6
6	IP ADDRESS 7	PORT NUMBER 7
7	IP ADDRESS 8	PORT NUMBER 8
8	IP ADDRESS 9	PORT NUMBER 9
9	IP ADDRESS 10	PORT NUMBER 10
10	IP ADDRESS 11	PORT NUMBER 11
11	IP ADDRESS 12	PORT NUMBER 12
12	IP ADDRESS 13	PORT NUMBER 13
13	IP ADDRESS 14	PORT NUMBER 14
14	IP ADDRESS 15	PORT NUMBER 15
15	IP ADDRESS 16	PORT NUMBER 16
16	IP ADDRESS 17	PORT NUMBER 17
17	IP ADDRESS 18	PORT NUMBER 18
18	UNDEFINED	
:		
31		

FIG. 11B

SRAM

ADDRESS	EN BIT (1 BIT)	CoS CHARACTERISTIC NUMBER (6 BITS)	INPUT PHYSICAL PORT NUMBER (4 BITS)	OUTPUT DESTINATION PHYSICAL PORT NUMBER (4 BITS)	CoS AREA (6 BITS)
0	1	0	0	3	3
1	1	1	0	3	1
2	1	2	0	3	2
3	1	3	0	4	1
4	1	4	0	5	3
5	1	5	1	6	1
6	1	6	1	7	3
7	1	7	3	0	1
8	1	7	3	0	2
9	1	7	3	4	4
10	1	8	4	1	1
11	1	9	4	1	4
12	1	10	4	6	1
13	1	11	4	6	1
14	1	12	5	1	1
15	1	13	6	1	1
16	1	14	7	4	1
17	1	15	7	7	1
18	0	UNDEFINED			
:	:				
31	0				

OF THE 32 TYPES, CHARACTERISTICS

TOTAL 32

INDICATES VALIDITY OF SET CONTENTS

CONTENTS OF CAM AND SRAM DATA IN ONE EMBODIMENT

FIG. 12A

(a) SMALLEST PARTITIONS OF CoS AREAS

START ADDRESS	END ADDRESS	PACKET BUFFER MEMORY
0000000h	01FFFFFh	0
0200000h	03FFFFFh	1
0400000h	05FFFFFh	2
0600000h	07FFFFFh	3
0800000h	09FFFFFh	4
0A00000h	0AFFFFFh	5
0C00000h	0CFFFFFh	6
0E00000h	0EFFFFFh	7
1000000h	11FFFFFh	8
1200000h	13FFFFFh	9
1400000h	15FFFFFh	10
1600000h	17FFFFFh	11
1800000h	19FFFFFh	12
1A00000h	1AFFFFFh	13
1C00000h	1CFFFFFh	14
1E00000h	1EFFFFFh	15
2000000h	21FFFFFh	16
2200000h	23FFFFFh	17
2400000h	25FFFFFh	18
2600000h	27FFFFFh	19
2800000h	29FFFFFh	20
2A00000h	2AFFFFFh	21
2C00000h	2CFFFFFh	22
2E00000h	2EFFFFFh	23
3000000h	31FFFFFh	24
3200000h	33FFFFFh	25
3400000h	35FFFFFh	26
3600000h	37FFFFFh	27
3800000h	39FFFFFh	28
3A00000h	3AFFFFFh	29
3C00000h	3CFFFFFh	30
3E00000h	3EFFFFFh	31

CoS UNIT NUMBER

FIG. 12B

(b) ACTUAL ALLOCATION FOR SRAM SETTINGS

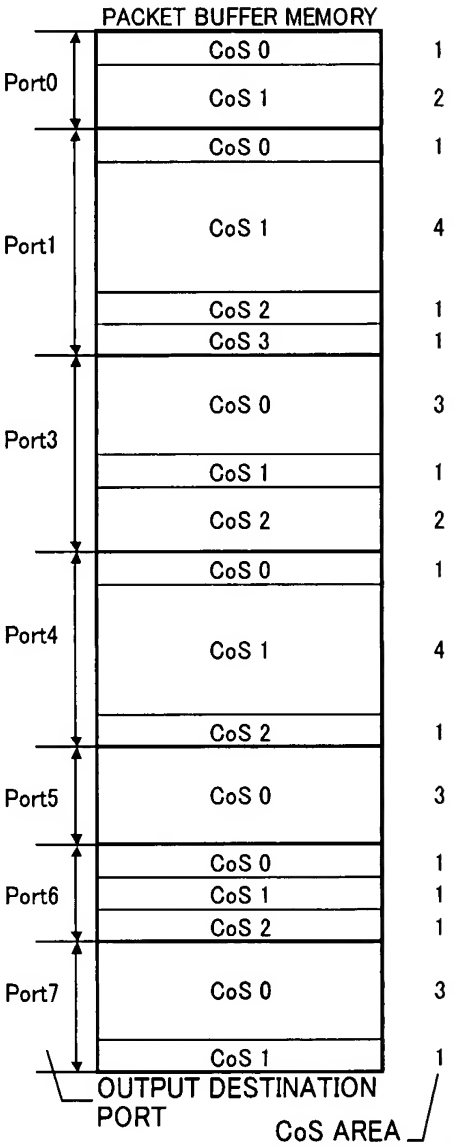


DIAGRAM OF ALLOCATION OF PACKET BUFFER MEMORY IN ONE EMBODIMENT

FIG. 13

No.	PACKET LOSS		ERROR INSERTION		PACKET DUPLICATION		DELAY INSERTION	
	EN	LOS FRACTION	EN	ERROR RATE	EN	DUPLICATION RATE	EN	DELAY TIME
0	0	–	0	–	0	–	1	100ms
1	0	–	0	–	0	–	1	1ms
2	0	–	0	–	0	–	1	50ms
3	0	–	1	10%	0	–	0	–
4	0	–	1	20%	0	–	1	100ms
5	0	–	1	30%	0	–	1	1ms
6	0	–	1	40%	0	–	1	300ms
7	0	–	1	50%	1	10%	1	1ms
8	0	–	1	50%	1	10%	0	–
9	1	10%	1	50%	1	10%	1	800ms
10	1	10%	1	50%	1	20%	0	–
11	1	10%	0	–	1	20%	0	–
12	1	20%	0	–	1	20%	0	–
13	1	20%	1	10%	1	20%	0	–
14	1	20%	1	20%	1	30%	0	–
15	1	20%	0	–	0	–	0	–
16	UNDEFINED							
:								
31								

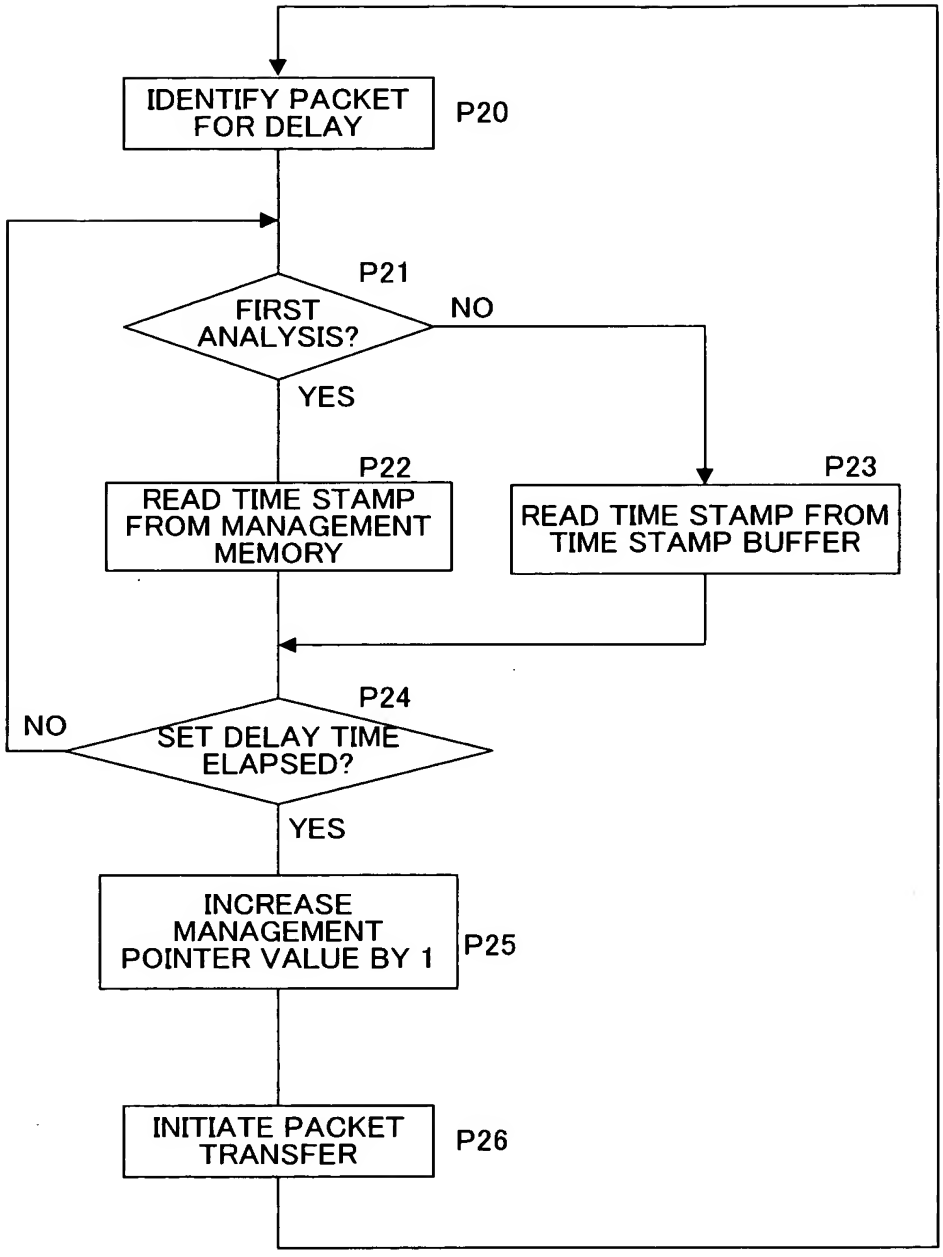
CONTENTS OF CoS CHARACTERISTIC TABLE IN ONE EMBODIMENT

FIG. 14

No.	OUTPUT DESTINATION PHYSICAL PORT NUMBER	DEQ CoS NUMBER	START ADDRESS	END ADDRESS	CoS CHARACTERISTIC NUMBER
0	0	0	0000000h	01FFFFFh	7
1	0	1	0200000h	05FFFFFh	7
2	1	0	0600000h	07FFFFFh	8
3	1	1	0800000h	0EFFFFFh	9
4	1	2	1000000h	11FFFFFh	12
5	1	3	1200000h	13FFFFFh	13
6	3	0	1400000h	19FFFFFh	0
7	3	1	1A00000h	1AFFFFFh	1
8	3	2	1C00000h	1EFFFFFh	2
9	4	0	2000000h	21FFFFFh	3
10	4	1	2200000h	29FFFFFh	7
11	4	2	2A00000h	2AFFFFFh	14
12	5	0	2C00000h	31FFFFFh	4
13	6	0	3200000h	33FFFFFh	5
14	6	1	3400000h	35FFFFFh	10
15	6	2	3600000h	37FFFFFh	11
16	7	0	3800000h	3CFFFFFh	6
17	7	1	3E00000h	3EFFFFFh	15
18	UNDEFINED				
:					
31					

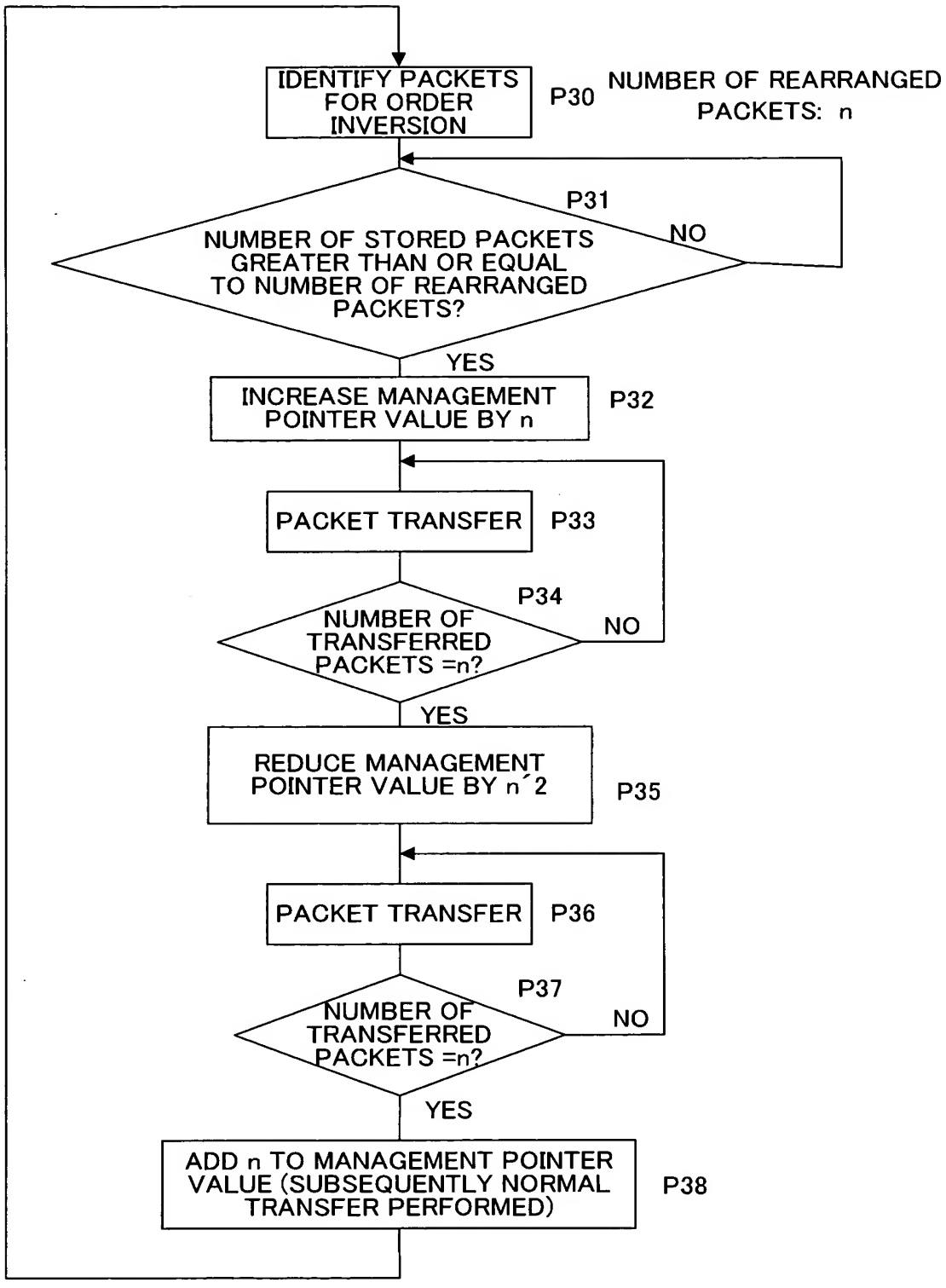
CONTENTS OF CONVERSION TABLE IN ONE EMBODIMENT

FIG. 15



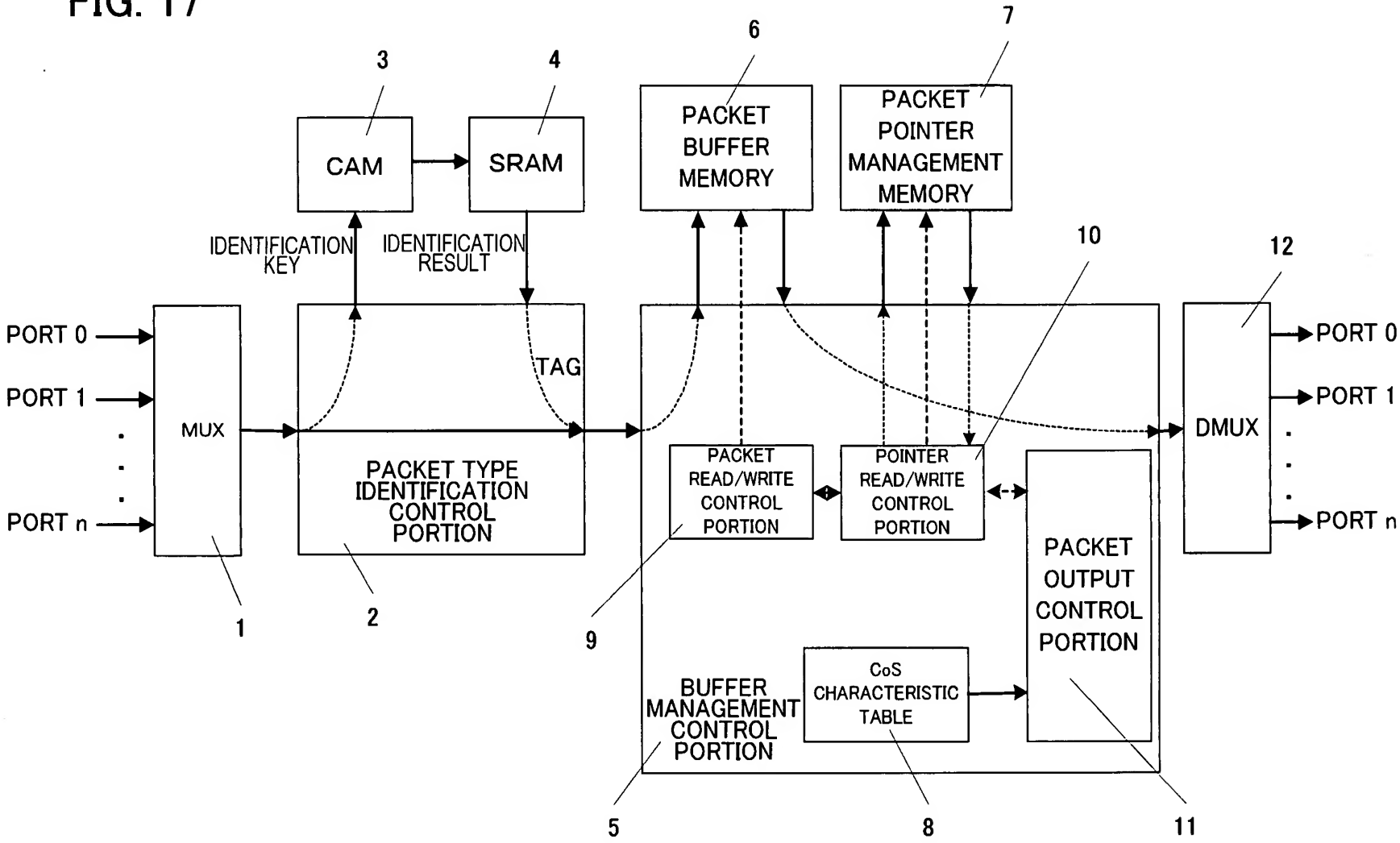
FLOWCHART OF OPERATIONS IN PACKET DELAY

FIG. 16



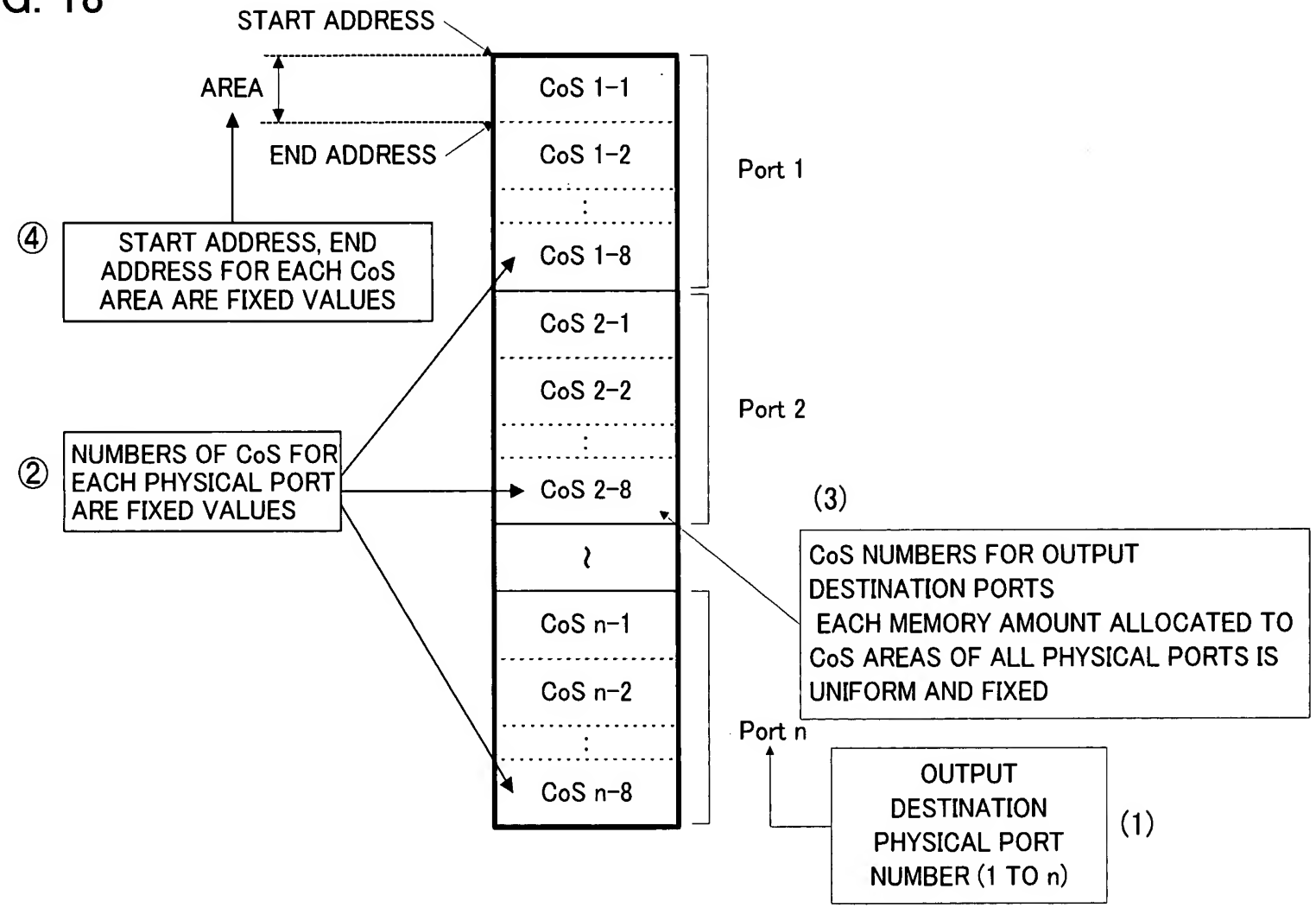
FLOWCHART OF OPERATIONS IN PACKET ORDER INVERSION/ REROUTING

FIG. 17



PRIOR ART

FIG. 18



PRIOR ART